## **EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	69240	((chip\$2 die\$2 ic integrated adj circuit\$2)near4(((array\$2 plurality first and second multi\$6) (row\$2 and column\$2)))same(substrate pcp board base))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:36
L2	69863	((chip\$2 die\$2 ic integrated adj circuit\$2)near4(((array\$2 plurality first and second multi\$6) (row\$2 and column\$2)))same(substrate pcb board base))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:58
L3	3148	((wafer)near4 (back rear bottom)) and 2	US-PGPUB; USPAT	OR .	ON	2006/12/21 22:49
L4	123	(perforat\$4 semi\$1cylind\$4) same((wafer)near4 (back rear bottom))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:50
L5	8	2 and 4	US-PGPUB; USPAT	OR	ON	2006/12/21 22:50
L6	2043	((chip\$2 die\$2 ic integrated adj circuit\$2)near4(stack\$5 cascad\$4 c\$1sod\$4)near4(substrate))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:40
L7	326	( (wafer)near4 (back rear bottom)) and ((via hole\$3)) same ((wall\$4) near5(insulat\$4 dielectric))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:41
L8	. 25	( (wafer)near4 (back rear bottom))same ((via hole\$3)) same ((wall\$4) near5(insulat\$4 dielectric))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:43
L9	4	6 and 8	US-PGPUB; USPAT	OR	ON	2006/12/21 22:43
L10	22	6 and 7	US-PGPUB; USPAT	OR ·	ON	2006/12/21 22:42
L11	291	( (wafer silicon substrate)near4 (back rear bottom))same ((via hole\$3)) same ((wall\$4) near5(insulat\$4 dielectric))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:59
L12	16	6 and 11	US-PGPUB; USPAT	OR	ON	2006/12/21 22:44
L13	14609	((wafer substrate silicon)near4 (back rear bottom)) and 2	US-PGPUB; USPAT	OR	ON	2006/12/21 22:58
L14	654	(perforat\$4 semi\$1cylind\$4) same((wafer silicon substrate)near4 (back rear bottom))	US-PGPUB; USPAT	OR	ON	2006/12/21 22:58
L15	65	2 and 14	US-PGPUB; USPAT	OR ·	ON	2006/12/21 22:50

## **EAST Search History**

L16	16837	((chip\$2 die\$2 ic integrated adj circuit\$2)near4(((array\$2 plurality first and second multi\$6) (row\$2 and column\$2)))same(substrate pcb board base))	EPO; JPO; DERWENT	OR	ON	2006/12/21 22:58
L17	660	((wafer substrate silicon)near4 (back rear bottom)) and 16	EPO; JPO; DERWENT	OR	ON	2006/12/21 22:58
L18	3	(perforat\$4 semi\$1cylind\$4) and 17	EPO; JPO; DERWENT	OR	ON	2006/12/21 23:00
L19	80	( (wafer silicon substrate)near4 (back rear bottom))and ((via hole\$3)) same ((wall\$4) near5(insulat\$4 dielectric))	EPO; JPO; DERWENT	OR	ON	2006/12/21 22:59
L20	55	(perforat\$4 semi\$1cylind\$4) and 16	EPO; JPO; DERWENT	OR	ON	2006/12/21 23:00